1. A method of fabricating a capacitor structure for a dynamic random access memory (DRAM), device, on a semiconductor substrate, comprising the steps of:

providing a transfer gate transistor on said semiconductor substrate, comprised of a gate structure on an underlying gate insulator layer, and comprised with a source/drain region located in an area of said semiconductor substrate not covered by said gate structure;

forming a conductive plug structure in an opening in an insulator layer, with said conductive plug structure overlying and contacting a portion of a top surface of a source region;

depositing an intrinsic polysilicon layer on the top surface of said insulator layer, and on the top surface of said conductive plug structure;

performing a series of ion implantation procedures at various implantation energies, to create ion implanted veins at different depths in said intrinsic polysilicon layer, with regions of said intrinsic polysilicon layer located between said ion implanted veins remaining as intrinsic polysilicon regions;

performing a dry etch procedure to define a storage node structure from said intrinsic polysilicon layer, with an isotropic component of said dry etch procedure selectively etching lateral grooves in said ion implanted veins, resulting in a necked profile, storage node structure featuring said lateral grooves in the sides of said necked profile, storage node structure;

forming a capacitor dielectric layer on said necked profile, storage node structure; and

forming an upper electrode structure on said capacitor dielectric layer resulting in said capacitor structure comprised of said upper electrode structure, of said capacitor dielectric layer, and of underlying, said necked profile, storage node structure.

2. The method of claim 1, wherein said insulator layer is a silicon oxide, or a boro-phosphosilicate layer, obtained via LPCVD or PECVD procedures, at a thickness between about 3000 to 12000 Angstroms.

3. The method of claim 1, wherein said opening in said insulator layer is formed via an anisotropic RIE procedure, performed using CHF_3 as an etchant for said insulator layer.

4. The method of claim 1, wherein said conductive plug structure is a polysilicon plug structure, obtained via deposition of an N type, in situ doped polysilicon layer via LPCVD procedures at a thickness between about 1000 to 7000 Angstroms, and defined via a chemical mechanical polishing procedure, removing unwanted portions of polysilicon from a top surface of said insulator layer.

5. The method of claim 1, wherein said intrinsic polysilicon layer is obtained via LPCVD procedures, at a thickness between about 3000 to 12000 Angstroms.

6. The method of claim 1, wherein said series of ion implantation procedures are performed at various implantation energies using either arsenic or phosphorous ions.

7. The method of claim 1, wherein said series of ion implantation procedures are performed using between about 3 to 10 specific energies.

8. The method of claim 1, wherein the lowest implantation energy used, resulting in the shallowest ion implanted vein in said intrinsic polysilicon layer, is performed at an energy between about 2 to 50 KeV, while the highest implantation energy used, resulting in the deepest ion implanted vein in said intrinsic polysilicon layer, is performed at an energy between about 50 to 100 KeV.

9. The method of claim 1, wherein the dose of implanted ions, used for the series of ion implantation procedures, is between about 2E13 to 7E17 atoms/cm^2.

10. The method of claim 1, wherein said dry etching procedure, used to define said necked profile, storage node structure, is performed via an inductive coupling plasma (ICP), procedure, with a top power for an ICP tool between about 100 to 1000 watts, a bottom plate at a power between about 30 to 300 watts, at a pressure between about 4 to 50 mtorr, and using an ambient comprised with Cl_2, HBr and He as an etchant.

11. The method of claim 1, wherein dry etching procedure results in a removal rate for said intrinsic polysilicon of between about 600 to 1000 Angstroms/min, while the removal rate of said ion implantation veins is between about 1000 to 2000 Angstroms/min.

12. The method of claim 1, wherein said lateral grooves in said ion implanted veins, formed during said dry etching procedure, are between about 50 to 500 Angstroms in length.

13. The method of claim 1, wherein the surface area of said necked profile, storage node structure is between about 2 to 4 times larger than a surface area for a flat surface, or a non- necked profile, storage node structure.

14. The method of claim 1, wherein said capacitor dielectric layer is a tantalum oxide layer, obtained via plasma vapor deposition procedures.

15. A method of fabricating a stacked capacitor structure for a dynamic random access memory (DRAM), device, on a semiconductor substrate, featuring a storage node structure comprised with lateral grooves located in the sides of said storage node structure, comprising the steps of:

providing a transfer gate transistor on said semiconductor substrate, comprised of a silicon nitride capped, polycide gate structure on an underlying silicon dioxide gate insulator layer, with insulator spacers located on the sides of said silicon nitride capped, polycide gate structure, and with a source/drain region located in an area of said semiconductor substrate not covered by said silicon nitride capped, polycide gate structure or by said insulator spacers;

forming a polysilicon plug structure in an opening in an insulator layer, with said polysilicon plug structure overlying and contacting a portion of a top surface of a source region;

depositing an intrinsic polysilicon layer on the top surface of said insulator layer, and on the top surface of said polysilicon plug structure;

performing multiple ion implantation procedures at various implantation energies, to create ion implanted veins, each located at a specific depth in said intrinsic polysilicon layer, and with regions of said intrinsic polysilicon layer, located between said ion implanted veins remaining as intrinsic polysilicon regions;

performing a dry etch procedure to define said storage node structure from said intrinsic polysilicon layer, with an isotropic component of said dry etch procedure selectively and laterally etching portions of said ion implanted vein regions exposed at the sides of said storage node structure, resulting in a necked profile, storage node structure featuring said lateral grooves in the sides of said necked profile, storage node structure;

forming a capacitor dielectric layer on exposed surfaces of said necked profile, storage node structure; and

forming a polysilicon upper electrode structure on said capacitor dielectric layer, resulting in said stacked capacitor structure comprised of said polysilicon upper electrode structure, of said capacitor dielectric layer, and of underlying, said necked profile, storage node structure.

16. The method of claim 15, wherein said insulator layer is a silicon oxide, or a boro-phosphosilicate layer, obtained via LPCVD or PECVD procedures, at a thickness between about 3000 to 12000 Angstroms.

17. The method of claim 15, wherein said polysilicon plug structure is comprised of situ doped N type, polysilicon, obtained at a thickness between about 1000 to 7000 Angstroms via LPCVD procedures, then defined via a chemical mechanical polishing procedure, removing unwanted portions of polysilicon from a top surface of said insulator layer.

18. The method of claim 15, wherein said intrinsic polysilicon layer is obtained via LPCVD procedures, at a thickness between about 3000 to 12000 Angstroms.

19. The method of claim 15, wherein said multiple ion implantation procedures are performed using either arsenic or phosphorous ions.

20. The method of claim 15, wherein the number of specific ion implantation procedures performed for said multiple ion implantation procedures, is between about 3 to 10.

21. The method of claim 15, wherein the lowest implantation energy used as part of said multiple ion implantation procedures, resulting in the shallowest ion implanted vein in said intrinsic polysilicon layer, is performed at an energy between about 2 to 50 KeV, while the highest implantation energy used with said multiple ion implantation procedures, resulting in the deepest ion implanted vein in said intrinsic polysilicon layer, is performed at an energy between about 50 to 100 KeV.

22. The method of claim 15, wherein the dose of implanted ions, used for said multiple ion implantation procedures, is between about 2E13 to 7E17 atoms/cm^2.

23. The method of claim 15, wherein said dry etching procedure, used to define said necked profile, storage node structure, is an inductive coupling plasma (ICP) procedure, performed using an ICP tool, with a top plate power between about 100 to 1000 watts, with a bottom plate power between about 30 to 300 watts, at a pressure between about 4 to 50 mtorr, and using an ambient comprised with Cl_2, HBr and He as an etchant.

24. The method of claim 15, wherein said dry etching procedure results in a removal rate for said intrinsic polysilicon of between about 600 to 1000 Angstroms/min, while the removal rate of said ion implantation veins is between about 1000 to 2000 Angstroms/min.

25. The method of claim 15, wherein said lateral grooves located in said ion implanted veins, formed during said dry etching procedure, are between about 50 to 500 Angstroms in length.

26. The method of claim 15, wherein the surface area of said necked profile, storage node structure is between about 2 to 4 times larger than a surface area for non- necked profile, storage node structure.

27. The method of claim 15, wherein said capacitor dielectric layer is a tantalum oxide layer, obtained via plasma vapor deposition procedures.